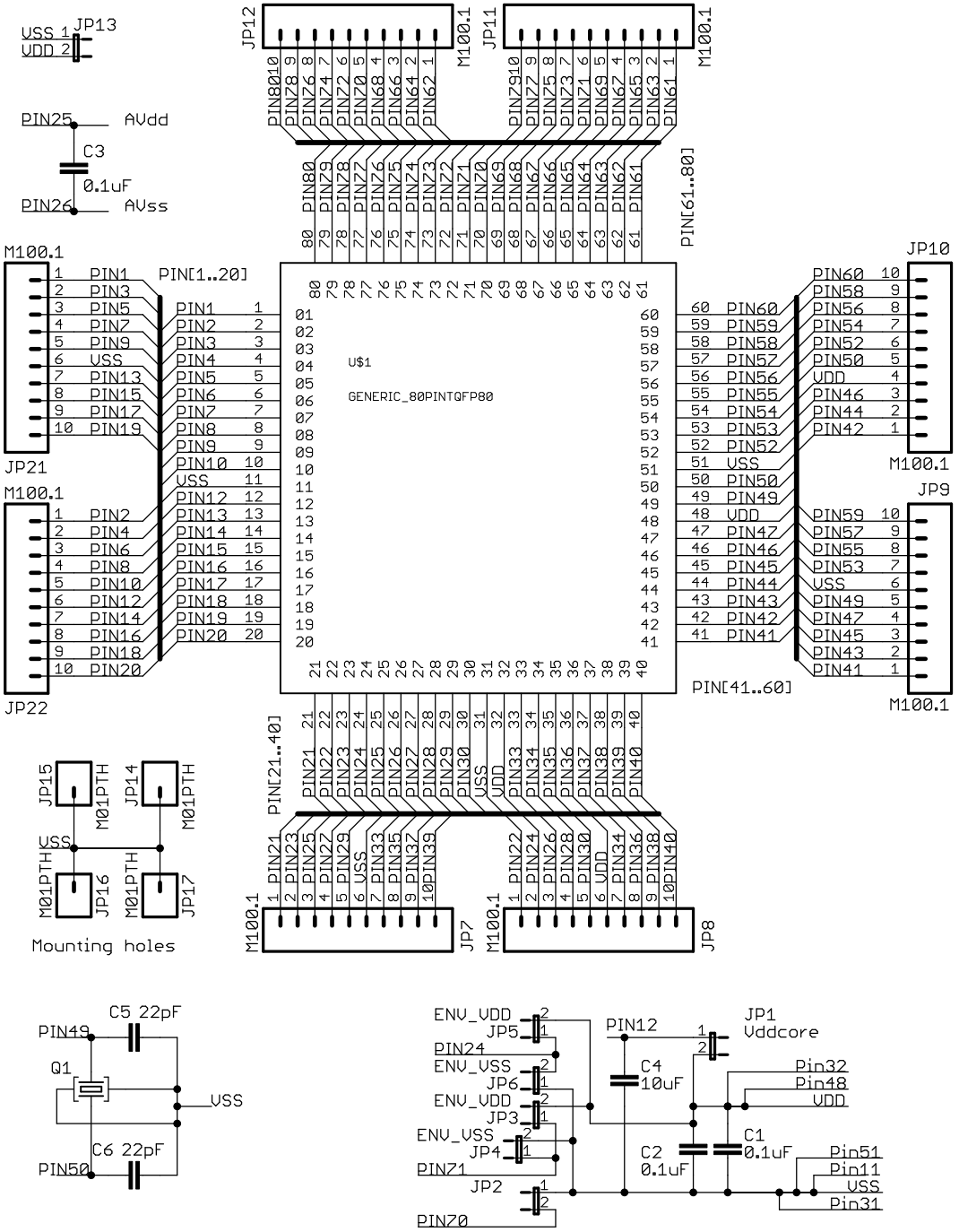

Power configuration

1. General
Never close JP3 and JP4, or JP5 and JP6, at the same time
It will short Vdd to Vss.

Vdd and AVdd are separate in each power configuration
Avdd has it's own bypass capacitor (C3)

2. Part specific

"Classic" PIC18s (PIC18F8722), dsPIC30F (dsPIC30F5013):
Close JP1, JP2, JP3; open JP4, JP5, JP6;
populate C4 with 0.1uF capacitor. Power from Vdd

J-series PICs (PIC18F83J1) 3 configurations are possible:
- Vddcore and Vdd are the same
(internal regulator is off, ENVREG tied to Vss)
Open JP4, JP5; close JP1, JP2, JP3, JP6;
populate C4 with 0.1uF capacitor. Supply Vdd (2.5V max).

- when using separate power sources for Vddcore and Vdd
(internal regulator is off, ENVREG tied to Vss)
Open JP1, JP4,JP5; close JP2, JP3, JP6;
do not populate C4. Supply Vddcore to Pin12, Vdd to Vdd.

- when using internal regulator to supply Vddcore
(ENVREG tied to Vdd)
Open JP1, JP4, JP6; close JP2, JP3, JP5;
populate C4 with 10uF ceramic cap. Supply Vdd to Vdd.

dsPIC33F (dsPIC33FJ64GP706)
close JP1, JP3; open JP4, JP5, JP6;
populate JP2 with 1uF ceramic cap, C4 with 0.1uF ceramic cap

PIC24FJ (PIC24FJXXGA008) 3 configurations are possible:
- when using internal regulator to supply Vddcore
Open JP4, JP5, JP6; close JP1, JP3;
populate JP2 with 10uF ceramic cap. Power from Vdd

- when using separate sources for Vdd and Vddcore
Open JP2, JP3, JP5, JP6; close JP1, JP4;
supply Vddcore on Pin70, Vdd on Vdd.

- when using same source for Vdd and Vddcore
Open JP2, JP3, JP5, JP6; close JP1, JP4;
connect Pin70 to Vdd

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